Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-9 (Canceled).

10. (Previously Presented) An integrated circuit device, comprising:
a substrate having at least one microelectronic device located therein; and
an insulating layer located over the substrate, including:
a thin-film, low-k dielectric layer having a first dielectric constant; and
a carbon nitride cap layer located on the low-k dielectric layer, wherein the carbon nitride cap layer has a second dielectric constant that is less than the first dielectric constant, such that the insulating layer has a third dielectric constant that is less than the first dielectric constant.

11. (Previously Presented) The device of Claim 10 wherein the thin-film, low-k dielectric layer has a first hardness and the carbon nitride cap layer has a second hardness that is greater than the first hardness, such that the insulating layer has a third hardness that is greater than the first hardness.

12. (Original) The device of Claim 10 wherein the cap layer has a composition of C_xN_y, where x ranges between 0.1 and 0.9 and y ranges between about 0.1 and 0.9.

13. (Original) The device of Claim 10 wherein the low-k dielectric layer comprises a material selected from the group consisting of:
silicon dioxide;
hydrogen-doped silicon dioxide;
fluorine-doped silicon dioxide;
carbon-doped silicon dioxide; and
an organic polymer.

14. (Original) The device of Claim 10 wherein the carbon nitride cap layer is a first carbon nitride cap layer formed on a first major surface of the low-k dielectric layer and further comprising a second carbon nitride cap layer contacting a second major surface of the low-k dielectric layer.

15. (Original) The device of Claim 10 wherein the carbon nitride cap layer is formed by a process selected from the group consisting of:

ALD;

CVD;

PECVD; and

PVD.

16. (Original) The device of Claim 15 wherein the carbon nitride cap layer is formed by a process gas selected from the group consisting of:

C_2H_4;

CH_4; and

C_3H_8.

17. (Original) The device of Claim 15 wherein the carbon nitride cap layer is formed by a process gas selected from the group consisting of:

N_2;

NH_3; and

N_2H_4.

18. (Original) The device of Claim 15 wherein the process is PVD utilizing a target comprising a material selected from the group consisting of:

graphite;

azaadenine;

adnine; and

melamine.

19. (Original) The device of Claim 10 wherein the carbon nitride cap layer has a thickness ranging between about 50 Angstroms and about 800 Angstroms.

20. (Previously Presented) An integrated circuit device, comprising:

a first via contacting a microelectronic device in a substrate and extending through a first insulating layer located over the substrate;

a first trench contacting the first via and extending through a second insulating layer located over the first insulating layer;

a second via contacting the first trench and extending through a third insulating layer located over the second insulating layer; and

a second trench contacting the second via and extending through a fourth insulating layer located over the third insulating layer;

wherein at least one of the first, second, third and fourth insulating layers includes:

a dielectric layer having a first dielectric constant; and

a carbon nitride cap layer located on the dielectric layer, the carbon nitride cap layer having a second dielectric constant that is less than the first dielectric constant such that the at least one of the first, second, third and fourth insulating layers thereby has a third dielectric constant that is less than the first dielectric constant.

21. (Original) The device of Claim 20 wherein an etch stop layer interposes at least one pair of neighboring ones of the first, second, third and fourth insulating layers.

22. (Original) The device of Claim 20 wherein at least two of the first and second vias and the first and second trenches form at least one dual-damascene structure.

23. (Original) The device of Claim 20 further comprising at least one anti-reflective coating formed over one of the first, second, third and fourth insulating layers.

24. (Original) A semiconductor device, comprising:

a plurality of doped regions formed in a substrate; and

a plurality of isolation regions each proximate a junction of adjacent ones of the plurality of doped regions, wherein at least a portion of each of the plurality of isolation regions comprises carbon nitride.

25. (Canceled).

26. (Previously Presented) The semiconductor device of Claim 24 wherein neighboring ones of the plurality of doped regions are oppositely doped.

27. (Previously Presented) The semiconductor device of Claim 24 wherein at least one of the plurality of isolation regions is selected from the group consisting of:

a field oxide region;

a local oxidation of silicon (LOCOS) region; and

a shallow trench isolation (STI) region.

28. (Previously Presented) The semiconductor device of Claim 24 wherein the carbon nitride has a composition of C_xN_y, where x ranges between 0.1 and 0.9 and y ranges between about 0.1 and 0.9.

29. (Previously Presented) The semiconductor device of Claim 24 wherein the carbon nitride is one of amorphous carbon nitride and polycrystalline carbon nitride.

Claims 30 and 31. (Canceled).

32. (Previously Presented) An integrated circuit apparatus, comprising:

a microelectronic device located at least partially in a substrate;

a dielectric first layer having a first dielectric constant and a first hardness; and

a second layer comprising carbon nitride and having a second dielectric constant and a second hardness, wherein:

one of the first and second layers interposes the substrate and the other of the first and second layers;

an aggregate dielectric constant of the first and second layers is less than the first dielectric constant; and

an aggregate hardness of the first and second layers is greater than the first hardness.

33. (Previously Presented) The integrated circuit apparatus of Claim 32 wherein the interposing one of the first and second layers contacts the substrate and the other of the first and second layers.

34. (Previously Presented) The integrated circuit apparatus of Claim 32 wherein the carbon nitride of the second layer has a composition of C_xN_y, where x ranges between 0.1 and 0.9 and y ranges between about 0.1 and 0.9.

35. (Previously Presented) A MEMs device, comprising:

a landing yoke configured to deflect in response to biasing thereof;

a mirror element coupled to the landing yoke; and

a control bus configured to bias the landing yoke;

wherein at least one of the landing yoke, mirror element and control bus includes a contact area coated with carbon nitride having a composition of C_xN_y, where x ranges between 0.1 and 0.9 and y ranges between about 0.1 and 0.9;

wherein a tip of the landing yoke is configured to contact the control bus in response to deflection of the landing yoke; and

wherein the tip is coated with carbon nitride.

36. (Previously Presented) The MEMs device of Claim 35 wherein a mirror support post interposes the mirror element and the landing yoke, and wherein the mirror support post includes a sidewall ring spacer comprising carbon nitride.

37. (Previously Presented) A MEMs device, comprising:

a landing yoke configured to deflect in response to biasing thereof;

a mirror element coupled to the landing yoke; and

a control bus configured to bias the landing yoke;

wherein at least one of the landing yoke, mirror element and control bus includes a contact area coated with carbon nitride having a composition of C_xN_y, where x ranges between 0.1 and 0.9 and y ranges between about 0.1 and 0.9;

wherein a mirror support post interposes the mirror element and the landing yoke; and

wherein the mirror support post includes a sidewall ring spacer comprising carbon nitride.